7. DSP IMPLEMENTATION

Using the Code Composer Studio software to do the simulations, this software uses the internal hardware of the DSP C64x+ very efficiently. The algorithms are implemented using DSP processor C64x+ and tested for different input data lengths. The following results are obtained for 10, 12 and 20 point DFT length; the clock cycle is equal to 1 GHz (1ns). We will compare the results found with the results in the paper [5]. Table 1 summarizes the resul1ts.

Table 1. The cycle's number, time taken and their ratios

Number of input sequences	DFT This work		DFT [5]		Ratio
	Benchmark (cycles)	Time taken (in ns)	Benchmark (cycles)	Time taken (in ns)	
10	372394	372394	24179	483580	1.3
12	556878	556878	28999	579980	1.04
20	1540534	1540534	96509	1930180	1.25

8. CONCLUSION

In this work we implemented a DFT using a DSP which is specialized in this kind of application, we can conclude that our implementation is faster (with a ratio of 1.3, 1.04, 1.25 for a number of sequences 10, 12, 20 respectively) compared work [5]. The results found leads us to conclude that the use of specialized circuits like the DSP will give better results than the use of circuits like FPGA which makes the implementation very expensive at the time level, architecture complexity.

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