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Electro Deposition of Nano Crystalline La2O3 on p-type Si Wafer and Electrical Characterization for CMOS Applications

K. Bikshalu[1], V.S.K. Reddy[2], P.C.S. Reddy[3], K.V. Rao[4]

[1]KU College of Engineering & Technology, Kakatiya University, Warangal-506009, India.
[2]Mallareddy college of Engineering and Technology, Secunderabad-500014, India.
[3]Jawaharlal Nehru Technological University Hyderabad , Hyderabad-500085, India.
[4] Centre for Nano Science and Technology, Institute of Science and Technology,
Jawaharlal Nehru Technological University, Hyderabad-500085, India
(kalagaddaashu@kakatiya.ac.in ; kalagadda2003@gmail.com)

Abstract

The present research work is divided into two parts namely (i). Electro deposition of nano crystalline thin films of lanthanum oxide or lanthana (La_2O_3) on silicon, (ii). Electrical characterization of deposited lanthana. Lanthana nano crystalline thin films are deposited on p-type silicon substrate by electrodeposition with precursor of Lanthanum nitrate ($La(NO_3)_3.9H_2O$) aqueous solution. Deposited lanthana thin films were characterized by, X-ray diffraction (XRD) for crystal structure determination, LCR meter for dielectric constant (K), Atomic force microscopy (AFM) and Scanning electron microscopy (SEM) for morphology studies.

Keywords: Electrodeposition of lanthana, Nano crystalline thin film, Nano lanthana, Electrical characterization, Lanthanum oxide.

1. Introduction

CMOS devices have high noise immunity and low static power consumption. Consequently, CMOS devices do not produce much heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip. Due to this reason CMOS won the race in the eighties and became the most used technology to be implemented in VLSI chips. The continued scaling of CMOS transistor requires replacement of the conventional silicon gate oxide (SiO2) or oxynitride (SiON) with a higher dielectric constant (K) for gate

dielectric to minimize the leakage current and to maintain a large capacitance for the drain current control. Among several contenders, the transition metal and the rare earth metal oxides, especially Lanthanum oxide (La_2O_3) and Hafnium oxide (HfO_2), are believed to be the suitable successors of the conventional gate dielectric material because of their several promising fundamental properties [1]. In this present work we have chosen the Lanthana because of its high contact stability with Si and high-K value and less equal oxide thickness (EOT) than the HfO_2 [2]. Lanthanum oxides exhibit some important applications like for example luminescent devices, sensors, up-conversion materials, and catalytic fields [3]. Lanthana also exhibits the diamagnetic properties [4]. Electrodeposition is the simplest and most economical method of preparing high quality metallic coatings, but it is rarely used to obtain oxide films. According to electrochemical thermodynamics (E-pH diagram), many active elements such as magnesium, aluminium, titanium, zirconium and rare earth elements cannot be deposited from aqueous or oxygen-containing organic solutions, but their oxides or other insoluble compounds can be easily deposited [5]. Platinum (Pt) electrode which we are using does not oxidize at any temperature [6].

2. Experimental

2.1 Electro deposition

Electro deposition method is simple and versatile when compared with Chemical Vapor Depostion, Physical Vapor Depostion , Pulsed Laser Depostion and Sputtering techniques. Electro deposition is divided into four steps. The four steps are specimens cleaning, solution preparation, electro deposition and annealing. Here specimens are the Pt and P-type Si vapors. Specimens are cleaned as per the process mentioned in Fig.1. Si substrate cleaning process is very important to realize desirable device performance, operation and its reproducibility. The wafers were cleaned by ultra sonication method using ultra pure water (UPW). Using UPW is most important because ultra pure water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. Firstly, a cleaning steps in solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2 = 4:1) performed to remove any organic material and metallic impurities for 5 minutes after UPW cleaning (10 min). The second step is cleaning wafers in a solution of dilute hydrofluoric acid (HF:H_2O=1:100) for 10 min to remove chemically and native oxides which might have been formed on Si surface. Specimens are dipped in UPW because to terminate hydrogen on

the surface for again10 min. Next one is the solution preparation. Add absolute alcohol (C_2H_5OH) and lanthanum nitrate in 0.05M (molar ratio) and stirring for 30 minutes. Finally solution and specimens are ready. Connect the negative electrode of the DC supply to the Si specimen and positive electrode to Pt metal specimen. Dip those electrodes in the solution at separation of 1 cm. Apply 5V to those electrodes for 1 second and collect Si specimen from the solution and dip in deionized water for removing the solution on deposited film. After electrodeposition the film material is lanthanum hydroxide (La(OH)3) and this film annealed at 9500c for 2 h to convert lanthanum hydroxide to lanthana and to stabilize in lanthana form [7].

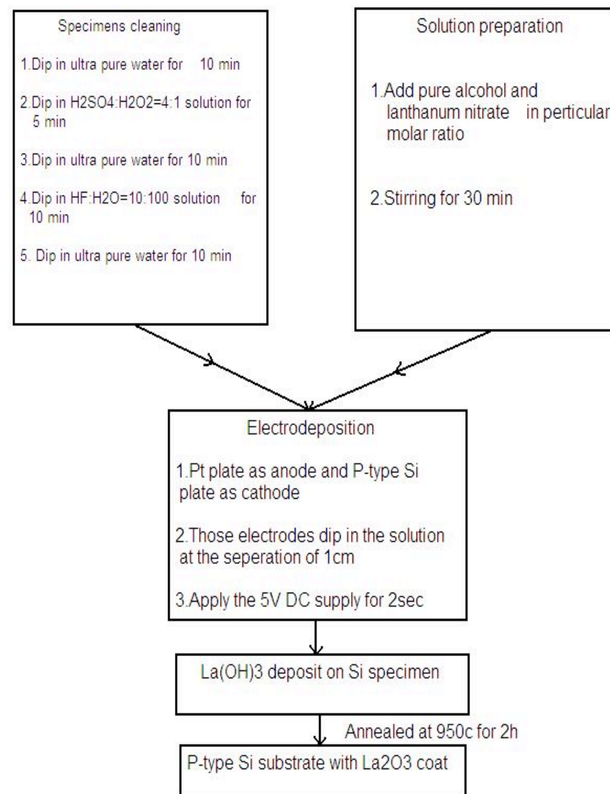


Fig. 1 Flow chart shows electro-deposition electro deposition of nano lanthana on P-type Si substrate.

3. Results and discussion

3.1. X-ray diffraction (XRD)

Crystallite size of deposited lanthana on p-type Si is 90nm (calculated from Fig. 2 and Fig.3). From the crystallite size nano crystallinity is observed in thin films. The variations of XRD pattern for different annealed temperatures are shown in Fig.2 and Fig.3. The dielectric constant (K) 25 was

observed by calculation from the knowledge of the capacitance (Cox), film thickness (d), the free pace charge permittivity (εo) and the area of the capacitor (A) using the relation K = Cd/ εo A.

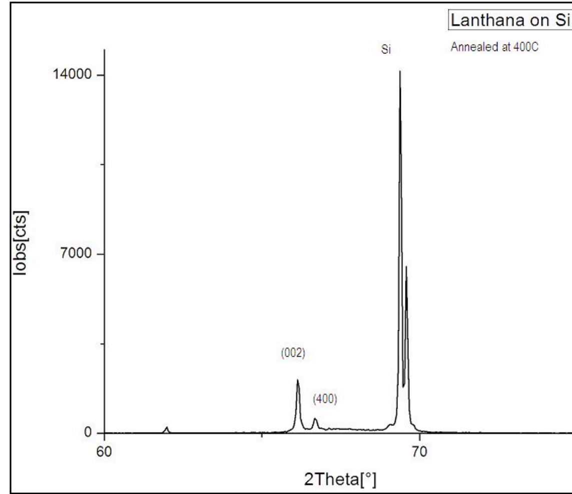


Fig. 2 XRD of deposited lanthana on p-type Si (annealed at 400^0C

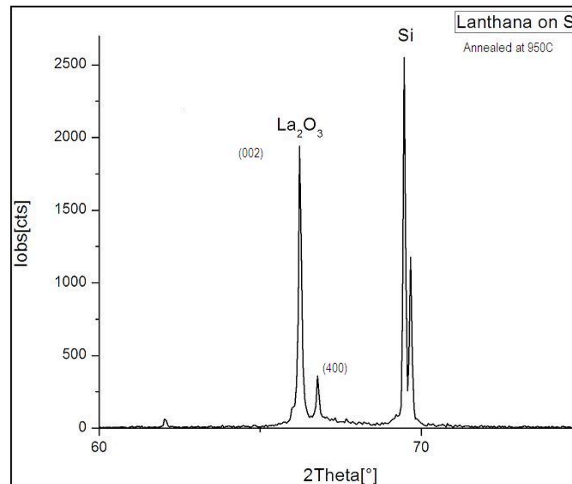


Fig. 3 XRD of deposited lanthana on p-type Si (annealed at 950^0C)

3.2. Atomic Force Microscopy (AFM)

Morphological analysis is performed with AFM analysis with A100 model (which is from A.P.E Research lab) in our laboratory. Best sample image has been shown in Fig.4

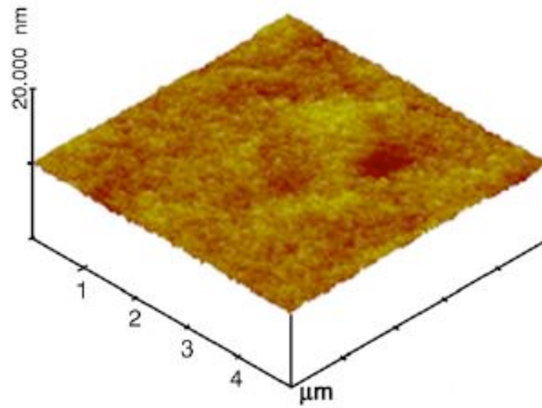


Fig. 4 AFM image of deposited nano crystalline La_2O_3 on Si

3.3. Scanning Electron Microscopy (SEM)

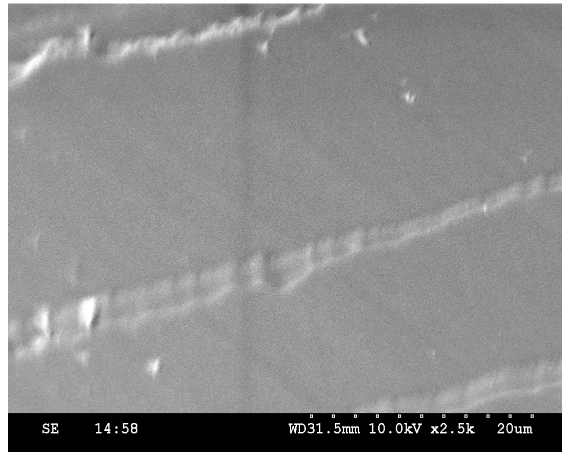
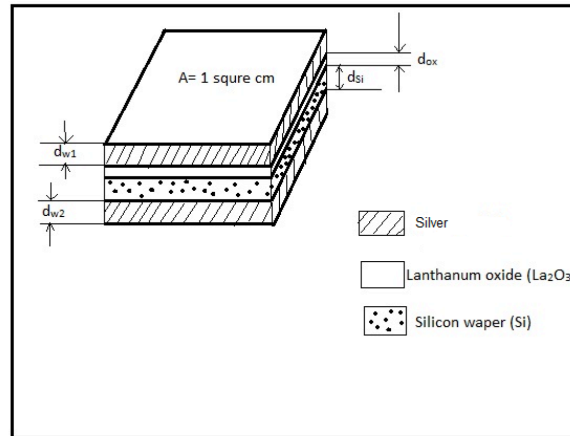


Fig. 5 SEM image of deposited nano crystalline La_2O_3 on Si

Another morphological analysis is performed with SEM analysis with Hitachi 3600 N model. In Fig. 5, SEM indicates the presence of layered lantha deposited with uniform thickness on Si wafer obtained by electro deposition technique.

3.4. Dielectric analysis

Dielectric analysis is done by E4980A model LCR meter at operating conditions of 1 kHz frequency. Initially metallization on the both side of the lanthana deposited Si wafer by RF sputtering. The Silver (Ag) metal is used for metallization. Final structure is shown in Fig. 6 (a). The Ag metalized lanthana/Si wafer equivalent circuit is as shown in Fig. 6(b).



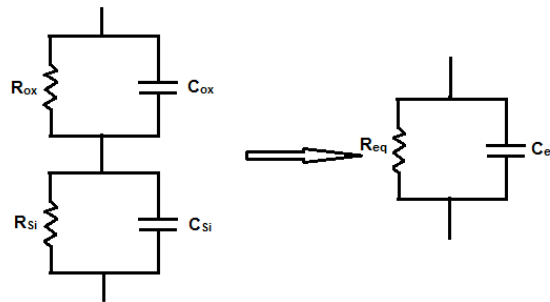


Fig. 6 (a) & (b) shows the Ag metalized Lanthana / Si wafer equivalent circuit

Here CSi is the capacitance of Silicon wafer and Cox is the capacitance of deposited lanthana on Si wafer and RSi is resistance due to Si wafer resistivity and Rox is resistance due to deposited lanthana resistivity. And the equation for capacitance is (shown in below).

$$C = \frac{\varepsilon A}{d} \tag{1}$$

Where C is capacitance, ε is permittivity of dielectric material (ε_o ε_r) and ε_o is permittivity of ambient air, ε_r is relative permittivity or dielectric constant of dielectric material, A is the Area of the film and d is the distance between the plates or thickness of dielectric material.

$$R_{eq} = \left(\frac{R_{si}.X_{si}^2}{R_{si}^2 + X_{si}^2} \right) + \left(\frac{\mathrm{R_{ox}}.X_{ox}^2}{R_{ox}^2 + X_{ox}^2} \right) \tag{2}$$

$$C_{eq} = \left(\frac{X_{si}.R_{si}^2}{R_{si}^2 + X_{si}^2} \right) + \left(\frac{\mathrm{X_{ox}}.R_{ox}^2}{R_{ox}^2 + X_{ox}^2} \right) \tag{3}$$

Where Rsi is the resistance due to resistivity of Silicon wafer, Xsi is the reactance due to dielectric nature of Silicon wafer, Rox is the resistance due to resistivity of deposited lanthana and Xox is reactance due to dielectric nature of deposited lanthana.

$$R = \rho \frac{1}{A} \tag{4}$$

Where R is the resistance, ρ is the resistivity, l is the thickness, Ais the area of the film Reactance

$$X = \frac{1}{(2\pi fC)} \tag{5}$$

Where f is the frequency (which is the LCR measure done), C is the Capacitance Here C_{eq} is the capacitance of total structure and R_{eq} is the resistance of total structure, which were calculated using LCR meter. R_{si} was calculated using ohm meter. Initially we know the values for C_{eq} as 31.716μF and R_{eq} as 3.355Ω, also area of deposited silver (A) is 1cm^2, thickness of silicon wafer is 625 µm, resistivity of Silicon wafer is 50Ωc.m, resistance of Si wafer R_{si} is 3.125Ω, dielectric constant of Silicon wafer (K_{Si}) is 11.7 and deposited lanthana thickness is 230 nm with resistance of deposited lanthana R_{ox} as 0.23Ω. Therefore, resistivity deposited lanthana is 10 kΩc.m.
Hence Dielectric constant of silicon wafer (K_{ox}) can be obtained by substituting the above measured and calculated values in the following equations (2) and (3); the resultant dielectric constant of deposited lanthana (K_{ox}) is measured to be 24.

4. Conclusions

Nanocrystalline La_2O_3 was successfully deposited on Si with a simple and versatile electro deposition technique. XRD analysis confirmed that the deposited nanocrystalline La_2O_3 has low crystallite size of 90 nm. AFM showed that deposited nano crystalline lanthana thin film with uniform surface morphology. SEM indicated the presence of layered lanthana with uniform thickness on Si wafer. The dielectric constant of deposited film of lanthana from the LCR meter analysis is 24. Further a metal coated on this nanocrystalline La_2O_3 deposited on silicon can be used as MOS capacitor and similarly after Ion implantation of this deposition, it can be used as a MOSFET.

5. Acknowledgement

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