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# Design Approach for Ultra Low Power Radiofrequency Analog Building Blocks

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## Abstract

This paper describes a new approach for ultra low power design of a radiofrequency building block in CMOS technology. This design approach is based on two parameters: First, the inversion coefficient of the transistor and the extracted equations from the radiofrequency circuits. Second, an optimum tradeoff between the performance key parameters such power consumption, gain, noise, linearity, geometry, etc. The effectiveness of this design approach has been demonstrated by a design example of a low noise amplifier in 130 nm CMOS technology at 2.4 GHz for Industrial, Scientific and Medical frequency band. The obtained results show that for just 545 μW of power consumption, the simulated gain of the LNA is equal to 13.5 dB and a noise figure of 1.5 dB with a good matching.

## Keywords

Inversion coefficient, design approach, CMOS, ultra low power, LNA, ISM

## 1. Introduction

Nowadays, the market of wireless sensor networks (WSN) is in full expansion. They have different applications that require nodes with low speed, low cost and very low consumption. Designing transceiver satisfying these constraints remains a challenge. The ZigBee standard, based on IEEE 802.15.4 is introduced to verify these constraints [1].

Currently, the CMOS technology is a good design choice because of its low cost, very high level of integrity and its high transit frequencies which reaches more than 100 GHz. Reducing power consumption while maintaining a good performance for the radiofrequency (RF) building blocks remains an interesting challenge in RF CMOS.

This work proposes a new approach for the design of an ultra low power low noise amplifier (LNA) in the Industrial, Scientific and Medical (ISM) frequency band. This approach is based on the inversion coefficient (IC) which represents a measure of the degree of inversion for a given device bias condition. IC = 1 represents the center of moderate inversion, while IC<< 1 indicates weak inversion and IC>> 1 signifies strong inversion. This design approach combines between the calculated equations issued from the RF circuit and the MOSFET coefficient inversion.

## 2. Description of the proposed design approach

The proposed design approach is based on the inversion coefficient which defines in detail the performance of the MOSFET in each operating regime from weak to strong inversion [2]. The biasing of the MOSFET transistor characterized by the drain current $I_d$ has a great influence on the performance of the LNA such as gain, noise and linearity. To explore the MOSFET transistor in all regions of operation, a method based on the inversion coefficient is developed in [2]. The expression of the inversion coefficient is defined in equation (1):

$$IC = \frac{I_d}{2n_0\mu_0 C_{ox} U_T^2 \left(\frac{W}{L}\right)} = \frac{I_d}{I_0\left(\frac{W}{L}\right)} \qquad (1)$$

Where $\mu_0$ is the low-field mobility, $n_0$ is the substrate factor, $C_{ox}$ is the gate oxide capacitance, $U_T$ is the thermal voltage, $I_0$ is the technology current, L is the channel length and W is the channel width.

Fig.1 shows the transconductance $g_m$ versus the inversion coefficient and Fig.2 shows the variation of the gate source voltage $V_{gs}$ versus the IC. These simulation results are obtained using 130 nm CMOS technology with L= 130 nm and W= 10 µm.

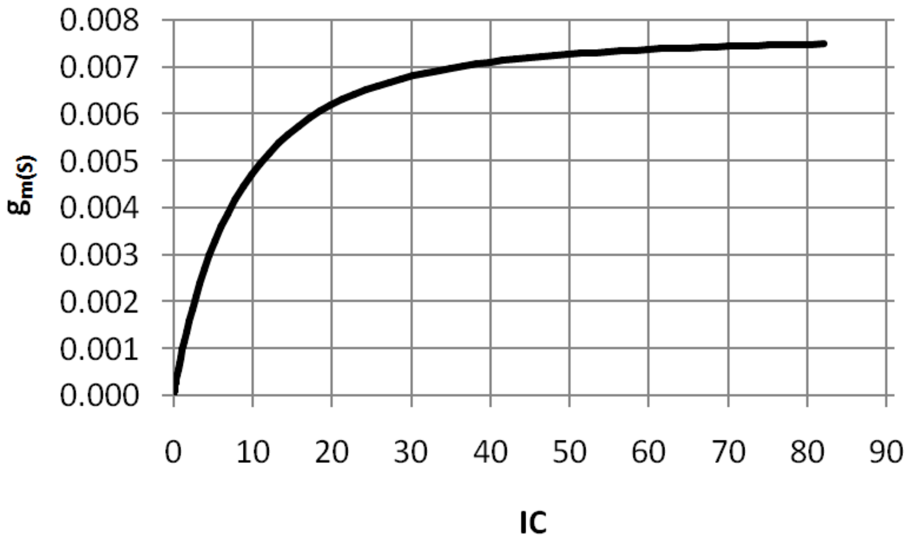


Fig.1. Transconductance versus inversion coefficient using 130 nm CMOS technology (L=130 nm, W=10 µm)

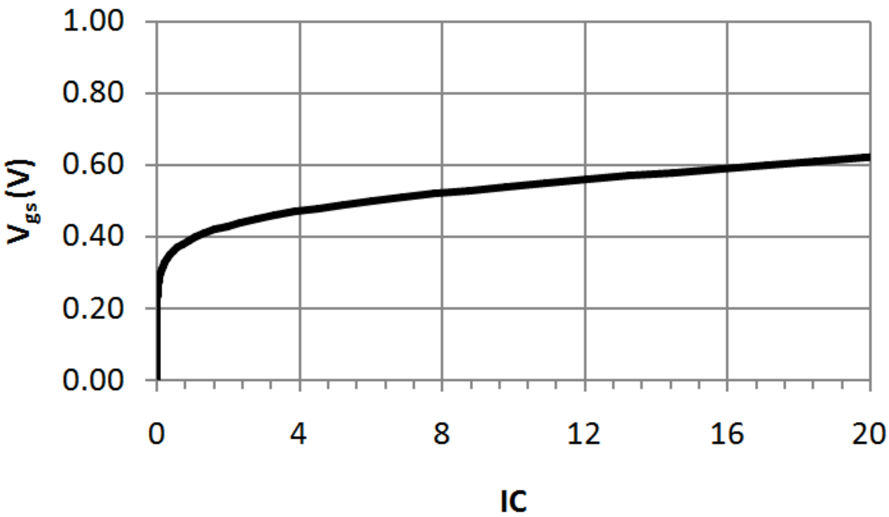


Fig.2. $V_{gs}$ versus inversion coefficient using 130 nm CMOS technology (L=130 nm, W=10 µm)

Three main regions of operation for the MOSFET can be defined limited by a fixed numerical value of the inversion coefficient. The subthreshold or weak inversion (IC <0.1) is characterized by low power consumption, a good gain and a maximum transconductance efficiency ($g_m/I_d$) but it suffers from low bandwidth. The region of strong inversion (IC> 10) is characterized by high power consumption, low $g_m/I_d$, low gain and excellent bandwidth. The moderate inversion region (0.1 <IC <10) is characterized by low power consumption, good gain, good transconductance efficiency and modest bandwidth. This last region represents an attractive choice for the design of ultra low power RF circuits.

Fig.3 shows the proposed design approach. Three degrees of design freedom are defined; the inversion coefficient, the channel length and the drain current ($I_d$). By selecting these three parameters, channel width is easily found. In addition to channel width, the passive components and the architecture of the RF circuit affect also the key performances such a gain, bandwidth, linearity, noise, etc. Combining between the inversion coefficient and the extracted circuit equations, an optimum trade-off can be found especially for ultra low power design.

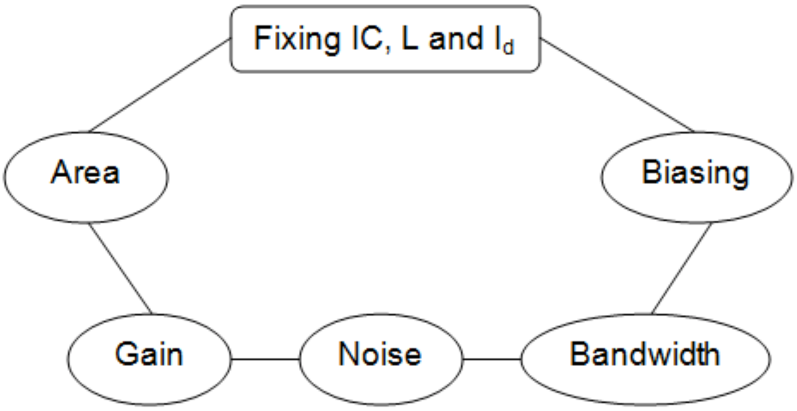


Fig.3. Design approach based on IC

## 3. Design example: LNA

The effectiveness of the proposed design approach is tested by designing a low noise amplifier. This interesting RF building block is the first stage of a receiver; its main function is to provide enough gain to overcome the noise of subsequent stages (such as mixers). The LNA should provide a good linearity, and should present specific impedance, such as 50 Ohms, both to the input source and to the output load. In addition, the LNA should provide low power consumption especially when it is used for wireless and mobile systems. At last, the LNA must have good reverse isolation to prevent self-mixing.

Fig.4 shows the topology of the LNA with inductive degeneration used for this design.

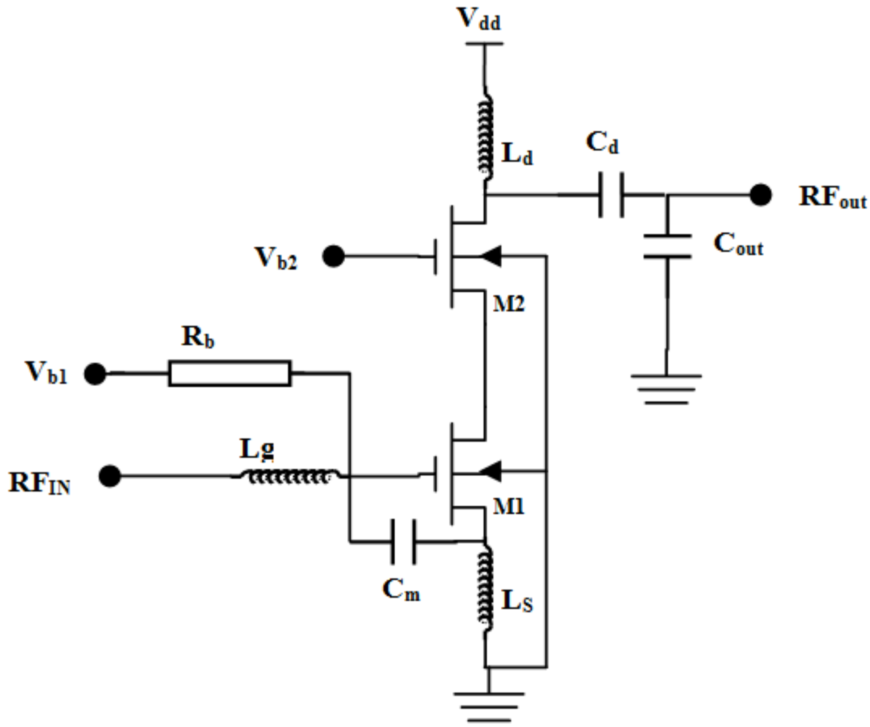


Fig.4. Topology of LNA used

This architecture has the advantage to achieve good input matching with power gain and noise for minimum power consumption [3]. The equation (2) gives the expression of the input impedance.

$$\begin{aligned} Z_{in} &= j\omega(L_s + L_g) + R_s + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \\ &\approx \omega_T\ L_s \approx \frac{g_m}{C_{gs}} L_s \qquad (\omega = \omega_0) \end{aligned} \tag{2}$$

The output load is an LC circuit tuned to the operating frequency $f_0$. However, the equation (3) shows the effective transconductance of the input stage. The expression of the noise figure which takes into account the series resistance of the gate inductance is given by equation (4) [4, 5].

$$G_{meff} = \frac{I_{in}}{V_{in}} = g_m Q_{in} = \frac{\omega_T}{2\omega_0 R_s} \tag{3}$$

$$F = 1 + \frac{R_{L_g}}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_{L_g}}\left(\frac{\omega_0}{\omega_t}\right) \tag{4}$$

Where, $\chi = \phi + \kappa = 1 + 2|c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_{L_g}{}^2\right)$

To design a LNA using the proposed approach for ultra low power applications, the designer should follow a procedure. The descriptions of the different design steps of the LNA are:

**Step 1:** Choosing the optimum RF architecture for low power design. This step is very important to avoid explicit power consumption drop. The chosen architecture is that of inductive degeneration (Fig.4).

**Step 2:** Fixing the desired performances: $NF_{max}$(maximum noise figure), $G_{min}$(minimum power gain), $IIP3_{min}$(minimum linearity) and $P_{max}$(maximum power consumption)). Table 1 shows an example of the desired performances for the design of the LNA.

| ***Parameters*** | **$NF_{max}$(dB)** | **$G_{min}$ (dB)** | **$IIP3_{min}$ (dB)** | **$P_{max}$ (µW)** | **$L_{max}$ (nH)** |
|---|---|---|---|---|---|
| ***Performances*** | 3.5 | 10 | -10 | 550 | 11 |

Table.1. Example of the desired LNA performances

**Step 3:** Extracting the active components which affect directly the LNA power consumption. The contribution of the second stage (M2) in terms of power consumption is very low. For this raison, we keep the transistor biased in the strong inversion region. Only the biasing of the transistor M1 determines the dc drain current $I_d$.

**Step 4:** Extracting the passive component which affect directly the LNA performances. For the inductive degeneration architecture, the integrated inductors and specially the series resistances of the inductors affect directly the noise figure and the 50 Ohm matching input impedance of the LNA. The use of a high quality factor $Q_{Lg}$ of the inductor is required. However, the value of the inductance L should kept lower than 11 nH as fixed in step 2.

**Step 5:** Simulation of the IC and selection of the three design parameters, IC, $I_d$ and channel length. The chosen parameters values depend on the desired performances fixed in step 2. Two parameters are already known, the channel length $L=L_{min}$ to provide high $f_T$ and $I_d=P_{max}/ V_{dd}$. Where $V_{dd}$ is the supply voltage, for $V_{dd}$=1 V the current drain is equal to 550 µA. From the performance of MOS transistor, the region near the center of moderate inversion (IC=1) represents a good tradeoffs in power consumption, gain, noise figure and bandwidth. For this raison we set IC=1.

**Step 6:** Setting the values of the parameters fixed in step 5 in the equations (1), (2), (3) and (4), the initial sizing of the LNA can be reached.

**Step 7:** Seeking for optimum tradeoffs in power consumption and others LNA performances through a series of simulations of various IC near the selected value IC = 1. Table 2 shows the optimum sizing of the LNA for 130 nm CMOS technology.

| **Parameters** | **Values** |
|---|---|
| W(M1) | 100 µm |
| L(M1,M2) | 130 nm |
| $L_g$ | 10 nH |
| $L_s$ | 1.2 nH |
| $L_d$ | 8 nH |
| $C_d$ | 0.48 pF |
| $C_{out}$ | 1.9 pF |
| $C_m$ | 0.243 pF |
| W(M2) | 90 µm |
| $V_{dd}$ | 1 V |
| $V_{b1}$ | 0.400 mV |
| $V_{b2}$ | 1 V |

Table.2. Sizing of the LNA for 130 nm CMOS technology

## 4. Results and discussions

Table 3 shows the simulation results obtained with 130 nm CMOS process for different values of IC. This table shows that the obtained gain reaches 10.7 dB with 1.89 dB of noise figure for just 360 µW of power consumption, while the other performances such as the third-order input intercept point (IIP3) and inductance value are respected. These performances continue to improve by increasing the inversion coefficient value but for more power consumption. The power gain reaches 15.34 dB with 1.4 dB of noise figure for only 750 µW of power consumption.

| *IC* | $V_{gs}$(V) | $I_d$(μA) | $g_m/I_d(V^{-1})$ | NF(dB) | gain(dB) |
|---|---|---|---|---|---|
| 0.60 | 0.46 | 360 | 20.16 | 1.89 | 10.7 |
| 0.73 | 0.47 | 430 | 19.6 | 1.66 | 12.12 |
| 0.89 | 0.48 | 525 | 19 | 1.55 | 13.35 |
| 1 | 0.49 | 629 | 18.5 | 1.46 | 14.42 |
| 1.3 | 0.5 | 750 | 17.9 | 1.4 | 15.34 |

Table.3. LNA performance for various IC values

Fig.5 shows the simulated LNA S parameters and noise figure using the 0.13 μm CMOS process. The reflections coefficients S11 and S22 are equal to -20 dB at 2.4 GHz ISM band for 13.5 dB of power gain.

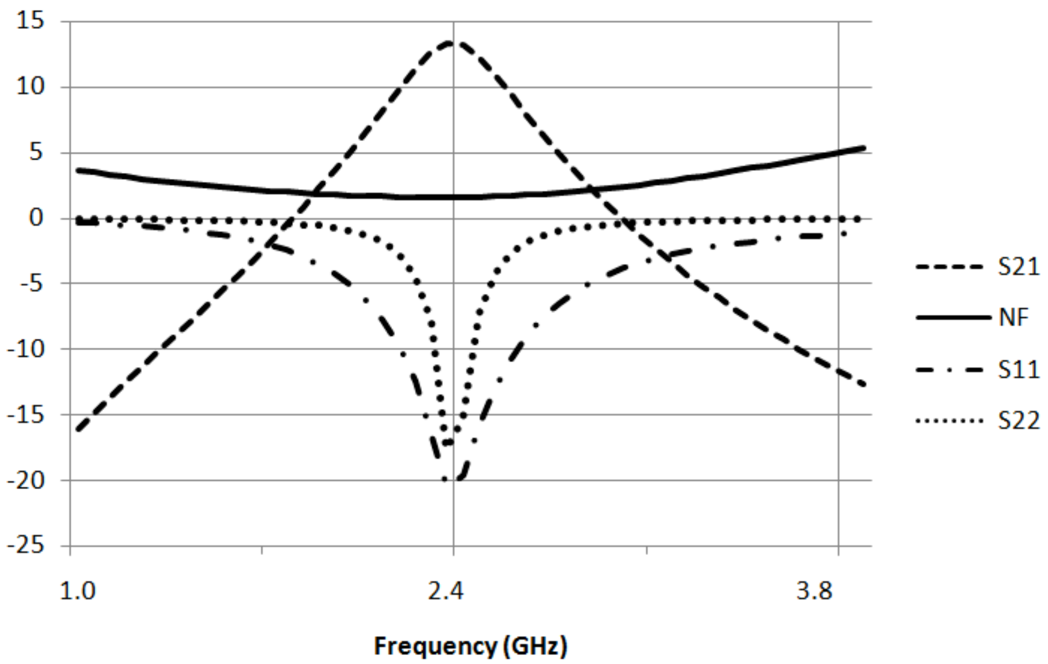


Fig.5. LNA S parameters and NF (dB) using 130 nm CMOS process

The simulated performance of the linearity defined by the 1 dB compression point (P1dB) is shown in Fig.6 for 130 nm CMOS technology.

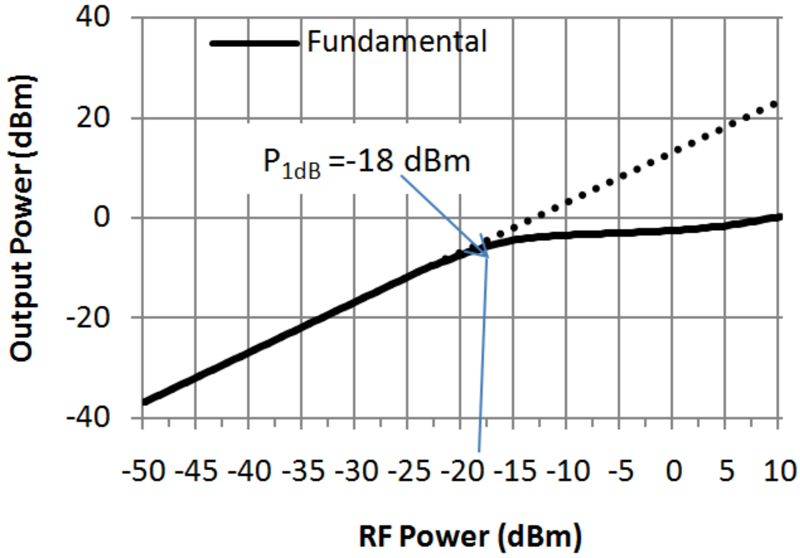


Fig.6. 1-dB compression point ($P_{1dB}$) using 130 nm CMOS process

Table 4 summarized the LNA performances in 130 nm CMOS process compared to the state-of-the-art. The LNA provides $P_{1dB}$ = -18 dBm and IIP3 = -9 dBm. In This work, the best performances of noise figure and power gain are achieved by comparing with other researches using different low power RF design techniques.

| **Parameters** | **This work** | **[6]** | **[7]** | **[8]** | **[9]** | **[10]** |
|---|---|---|---|---|---|---|
| Year | | 2007 | 2008 | 2009 | 2011 | 2013 |
| f (GHz) | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | 3.66 |
| NF (dB) | 1.5 | 2.8 | 5.2 | 2.2 | 3.85 | 2 |
| Gain (dB) | 13.5 | 22.7 | 21.4 | 14.4 | 10.7 | 14 |
| Power (μW) | 533 | 943 | 630 | 1700 | 570 | 2800 |
| $S_{11}$ (dB) | -20 | -14 | -19 | -23 | - | -10.6 |
| $S_{22}$ (dB) | -20 | - | - | -13.7 | - | - |
| $V_{dd}$ (V) | 1 | 1 | 1 | 0.4 | 1 | 0.8 |
| IIP3 (dBm) | -9.5 | 5.14 | -11 | - | -5 | 10.5 |
| $P_{1dB}$ (dBm) | -18.5 | -10 | -15 | -15.45 | - | - |
| Technology | 0.13 | 0.09 | 0.18 | 0.13 | 0.09 | 0.13 |

Table.4. Comparisons of LNA performances with the state of the art

## 5. Conclusion

A new design approach for RF circuits has been described. The sizing of the circuit components is performed by the use of the inversion coefficient. The main advantage of the proposed design approach is the time reduction by seeking the initial sizing of the RF building blocks. The big challenge in this work is to reduce the power consumption to µW values while satisfying the requirements of IEEE 802.14.5. The technique consists of biasing the transistor in the moderate inversion and then finding the right compromise between power consumption and the most RF performances. The obtained results are acceptable for low power RF standards especially for the IEEE 802.15.4. Therefore, this design approach can be used in the design of others building blocks of a RF transceiver to ensure optimized power consumption without dropping others performances.

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