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Performance Evaluation of a Multi-Sensor System using Fixed Point DSP for Water Leak Detection

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Abstract

DSPs (Digital Processors Signal) are processors specifically designed for digital signals processing. The fixed-point DSPs are processors operating in integer arithmetic whose characteristics are often limited but not less powerful with respect to floating-point DSPs. In this article, it is a question of checking the performances provided by the fixed-point DSP, the TMS320C541. This one is used in a detection and remote locating system ensuring a control of water leaks on the pipes. The acoustic correlation technique used as means of detection of these leaks represents the key element of the suggested system. In fact the DSP which deals the acquisition and processing of the signals emanating from the leaks. The had aim consists in initially to confirm the choice of such a processor for such an application. A simulation study to evaluate its performances as regards of computational accuracy and computing speed is carried out. A floating-point DSP of last generation, more accurate and faster, taken as reference element, is used for this purpose.

Keyword:

Acoustic Correlation, fixed-point DSP, floating point DSP , calculation accuracy, computation speed, Simulation.

1. Introduction

The DSPs with their architectures and their instruction sets specially adapted to the signals processing algorithms, very often represent a better compromise compared to the other integrated solutions [1]. The Fixed-point DSPs by far are used, mainly for their lower cost, to the detriment of an accurate calculations check, and of a development time fairly consistent. Their programming specifically in assembly language, among other things allows them to reach

important computing speeds relatively to the floating processors which are often faster, more accurate, but also more expensive.

The aim in this article consists in evaluating the performances of calculation of the fixed-point Texas Instruments, the TMS320C541. This one functioning at a speed of 50 MHz, is located at the heart of processing unit of a multisensor system of detection and remote localization of water leaks [2]. The detection principle used in this application is containing acoustic signals emanating from leaks located remotely on pipes. Of socio-economic interest, this system is expected to be used in wide field exploitation, where it is judicious to control a large number of pipes. The selected DSP must answer the criteria of speed, lower cost, and extension (multiprocessor support). The performances as regards of cost, of accurate of calculation, and computing speed, are the principal arguments which plead in favour of a judicious choice of the DSP in question.

It is presented in this work the performance evaluation of the DSP chosen for the suggested system. An analysis of the accuracy of calculation, of capacity of acquisition and processing of the system, is presented. The criteria of selection and choices used by the originators and researchers are first presented.

2. Choice of the DSP

It should be said first that the choice of this type of processors strongly depends on the application selected. To this end, one can consider while choosing such or such processor, a certain number of factors which change from one to another [3, 4]. The performances criteria used by the specialists to select a DSP intended for a given application, can be quoted as follows.

2.1 Arithmetic calculation

One of the most fundamental characteristics of a DSP processor is the kind of arithmetic related to its architecture. For fixed-point DSPs, the programmer must imperatively and carefully to measure with various stages of the program, the numerical accuracy proportioned with the imposed limited dynamic range [3, 4]

2.2 Dynamics of the words

The bit size which represents the dynamics of a word has an important impact on the cost. It is in close relationship to the accuracy of calculation which must be absolutely verified.

2.3 Computing speed

Another standard measurement for the choosing of a DSP processor in a given application is the computing speed. There are various ways of measuring this one. The MAC operation can be used as basic measurement to evaluate the computing speed. It is to be stressed that this one is carried out in only one cycle of instruction in the DSP C541. Faster, C6701 executes 5 times rather more MAC operations in only one instruction cycle [5, 6].

2.4 Organization of the memory

The organisation of the memories can have a great impact on the functioning of DSPs. The presence of hiding memory can be only essential for this type of architectures, in order to make it possible the instructions to seek the words locally and not outside.

2.5 Facility of development

The degree of facility of programs development depends on the application in question, and the choice of a DSP depends rather on the software tools used. The floating-point DSPs tend to comprise regularly more of instructions and are thus less restrictive than fixed-point DSPs. They have a code which remains always less optimized and this, whatever the degree of optimization of the program realized. The use of a fixed-point DSP programmed in assembler language can present better performances at the detriment of a more significant development time.

2.6 Multiprocessor support

Some high flow applications to requiring of complex calculations often require the parallel use of several DSPs. This multiprocessor support is appropriate enormously for systems open to possible extensions.

2.7 Power consumption

The power of DSP can change from one moment to another according to the instructions it executes. This parameter evoking the power consumption is essential to evaluate for embedded applications or applications requiring the exploitation of several prototypes used on a large scale[7].

2.8 Cost

Obviously the cost of the processor is a major concern for the products produced in series. The DSP TMS320C541 is relatively less expensive compared with the floating-point DSP, the DSP C6701. Its price, 5 to 10 times lower, represents an essential economic aspect for a system having to be used on a large scale.

The TMS320C541 chosen in this application is regarded as the first member of the TMS320C54x family of fixed-point DSPs of 16 bits. It largely checks the widely all the already selection criteria. The architecture of this type of processors presents in fact an important improvement compared to the preceding ones C2x and C5x. Only, the peripherals and the interfacing remain traditional [8]. The basic architecture type is Harvard modified, including a bus for the memory programs, three bus for the data memory and four adress bus. Those provide access it possible to reach 64 kwords of program memory, 64 kwords of given memory and 64 kwords of input/output, is a total of 192 kwords. The simultaneous access to the program and the data makes it possible to parallel operations. There are three readings and a writing in memory which can be performed out in the same cycle time [9].

The study of the architecture of the processor makes it possible to see the high parallelism of the central processing unit (CPU). It includes a MAC consisting of a multiplior and a 40 bits adder; an arithmetic logic unit (ALU) that can perform 40 bits being able to carry out various arithmetic operations and manipulation of bit, whose result can be stored with the choice in one of the two 40 bits accumulators [9].

3. Architecture

The multisensor system of acquisition and processing intended to supervise the remote water leaks is presented in figure 1. The signals emanating from these leaks are transmitted from sensors (microphones) towards a control station having a master-slave architecture structured around four principal parts:

- A reception and collection system of the signals playing the role of demodulator.
- An acquisition interface, multiplexing and A/D conversion, lying out with a flash ADC of 8 bits resolution.
- A coprocessor card based of TMS320C541 DSP, playing out the role of slave, and who ensures the data acquisition and their processing.
- A host PC playing the role of the Master, allowing the entry of the operating parameters, the data display, the saving and printing of the results obtained.

3.1 Acquisition

The circuit of the acquisition interface is indicated in figure 2. One shows the presence of a dialogue between the Master (PC) and slave (DSP) ensured by 04 signals of communication used to allow the exchange of the operating parameters and the data. Multichannel acquisition is ensured by the DSP under the control signals of interruption INT0 and INT1 coming from the timer. Those related to interruptions IRQ0 and IRQ1 of the DSP, a control of addresses generator (counter) for the signals multiplexing. Those are acquired at the level of a RAM extension memory of 8M x16 bits, exploitable by pages of 1k x16bits through a window called : interest area [10].

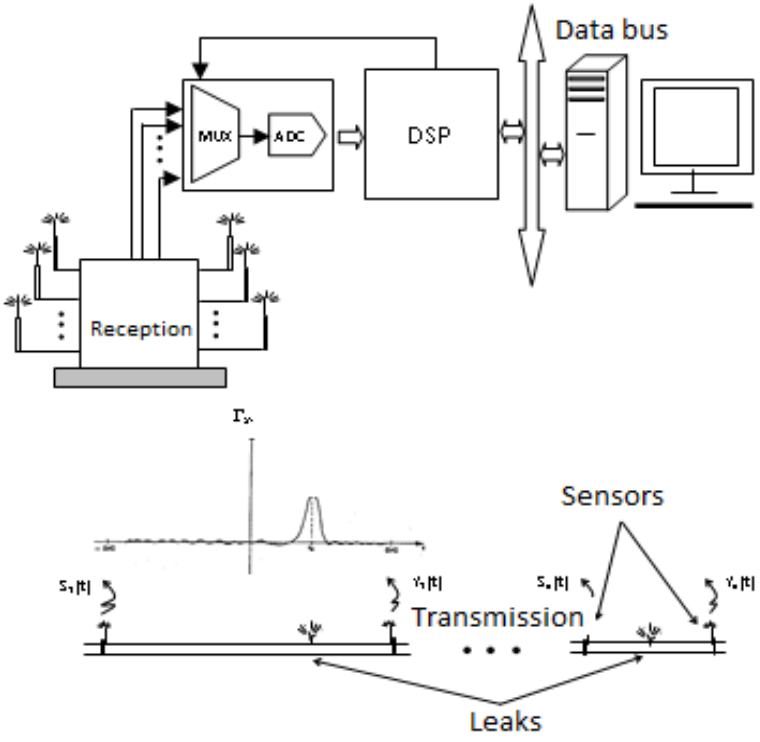

Figure 1: Multi-sensor system for leaks detection.

We have the following relation [10]:

$nF_{max} = f_{mux}/k$ (1)

one again :

$n = 1/k \, . \, f_{mux} / F_{max}$ (2)

with:

F_{max} = maximum frequency of the input signals,

f_{mux} = multiplexing frequency ,

k = factor of sampling.

After the DSP finished the acquisition and the processing of the acquired signals, the PC preceded the data transfer for display data, safeguard, and decision-making possible.

3.2 Processing

The correlation technique is the calculation algorithm used like means of detecting leaks in the system presented. We must confirm the choice of the DSP used while preceding the test of its performances as regards accuracy of calculation and processing speed. The correlation function used is given according to the following relation:

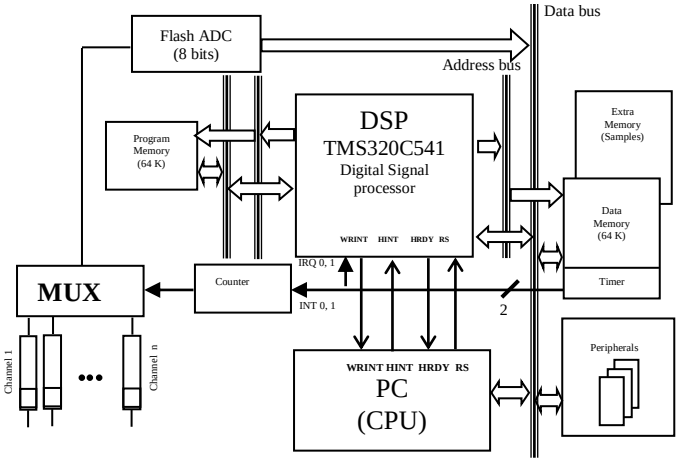

Figure 2: Acquisition interface circuit.

$$\Gamma_{SY}(K) = \frac{1}{N-K}\sum_{n=1}^{N-K} S_q(n)Y_q(n+K) \quad \begin{cases}(1 \le n \le N-K)\\(0 \le K \le M \prec N)\end{cases} \quad [11]. \qquad (3)$$

The algorithm constructing this function is demanding in computing times, considering the significant number of MAC operations used. With an aim of comparative, the algorithm is established at the same time on the DSP C541, the DSP C6701 and on the PC. C541 is programmed in assembler language; whereas C6701 and the PC are programmed in C language. We evaluate the processing speed and the acquisition duration of the system.

The principle of multiplexing flash operated at the acquisition interface leads to following relation:

$$T_{acq} = \frac{N_s}{n \times F_s} \qquad (4)$$

Such as:

N_s = number of samples acquired in memory.

F_s = sampling frequency of input signals.

T_{acq} = acquisition duration, necessary to the filling of the memory.

n = number of channels selected in entry.

According to this principle of acquisition, a significant number of channels can be multiplexed in entry. The limitations milked only with the extension memory available on the DSP.

4. Performance Evaluation

4.1 Accuracy

In order to evaluate in an experimental way the accuracy of calculation of the DSP (16 bits) used, a direct comparison with the results provided by the PC (32 bits) is operated. The evolution of the relative error ($RE = \frac{|PC - DSP|}{PC}.100\%$) of calculation is shown on figure 3.

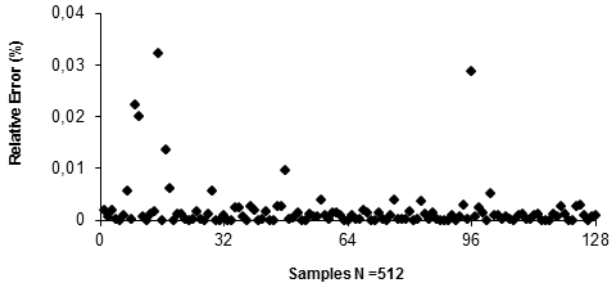

Figure 3: Evolution of the calculation relative error.

The variation of this error is concentrated in the range 0-0.01%. A largely sufficient accuracy despite the calibration of the input data. An explanation can be given for this purpose, which consists in saying that MAC with 40 bits of the DSP is due principal cause. Indeed, all the MAC operations are carried out with round-off. More especially as the capacity overshootings did not take place because of the dynamics of the words reduced to 1/N.

4.2 Speed

With the aim of evaluation of this processor in terms of computing speed, a comparative study is operated with the DSP C6701, as well as the PC which functions at 2.42 GHz. The results obtained are shown in table1.

N (Samples)	C541 (ms)	C6701 (ms)	PC (Pentium IV) (ms)	C6701/C541	PC/C541	C6701 / PC
256	3.82	0,32	0.93	11.68	4.10	2.85
512	6.88	1,25	3.46	5.49	1.98	2.7
1024	19.19	4,92	13.18	3.89	1.45	2.68
2048	68.40	19,58	51.81	3.49	1.32	2.64

Table1. Computing time of the 3 processore

In terms of computing speed, it appears according to the results obtained that the floating DSP C6701 is fastest. It is faster of 2.6 times than the PC dispite of the important speed of this one (more than 14 times).

However this DSP is only of 3.5 times faster than C541, knowing that this last has a speed of operation of 3.3 times lower. In more of lower cost, the results show clearly that the two performance criteria, namely the accuracy of calculation and the processing speed, are checked for the DSP C541. In off-line, and for a time of acquisition 10 times lower than the processing time, the system are able to supervise 30 leaks simultaneously. That is to say 2 hours of discontinuous control per day.

4.3 Discussion

The results shown in the table below table2 evoke the optimization character of the program carried out. The DSP C541 executes a highly optimized code with a ratio of 2.6 between the theoretical and real elementary execution times of a MAC operation. Despite its high performance hardware characteristics of five (5) MACs, the number of multipliers / accumulators it has, the floating DSP C6701 performs a less optimized code with a ratio of 18.6. An optimization rate of the code executed by the C541 can be ciphered at 7 times relatively better at C6701. This probably explains the speed performance achieved by the fixed-point DSP.

DSP	Elementary execution time of one MAC operation (ns)		Number of MACs	Language	Code
	Theoretical	Real			
C541	25	65.23	1	Assembleur	Very optimized
C6701	1	18.6	5	C	Less optimized
PC	-	49.41	-	C	Not Optimized

Table2. MAC execution time (ns)

Conclusion

Justifying of a more economic cost and increased performances, the TMS320C541, was thus selected to function in a multisensor system of leaks detection. Its performances evaluated as regards capacity of acquisition and processing were well checked. The results obtained in terms accuracy of calculation and processing speed were considered to be very satisfactory. The characteristic of multiprocessor support which this DSP enjoys opens in fact other horizons of extension and exploration on a large scale. With these performances, a on-line processing operating on a more significant number of input channels, remains possible. They can be improved more if one uses other processors at fixed point of the same family, having a speed of higher clock. As an indication, DSP TMS320C549 has a speed of clock of 100 MHz. a fixed-point DSPs of last generation of the C64xx family can play a decisive part in this type of application.

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